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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,972	06/25/2001	Yoshihisa Kato	740819-566	7056

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EXAMINER
PHAM, LY D

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/886,972	Applicant(s) KATO ET AL.	
	Examiner Ly D Pham	Art Unit 2818	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) *3 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL ACTION

DETAILED ACTION

Election/Restrictions

1. Claims 3 – 4 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention(s), there being no allowable generic or linking claim. Election was made **without** traverse as indicated in the previous Office Action.

2. Applicants' Amendment A has been entered in Office paper No. 5, dated October 08, 2002.

Claim Rejections - 35 USC § 102

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Taira (US Pat 6,049,477).

Claim Rejections - 35 USC § 103

4. Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taira in view of Ishiwara (US Pat 6,362,500 B2).

5. Rational for the rejections of claims 1 and 2 have been addressed in the previous Office Action, dated June 14, 2002.

Response to Arguments

6. Applicant's arguments filed in October 08, 2002 have been fully considered but they are not persuasive.

Contrary to applicants' argument regarding claims 1 and 2, the reference by Taira has shown the feature of "setting a magnitude of the voltage applied between the drain and the source of the FET in the step of reading a data, within the range where the drain-source current of the FET increases as the drain-source voltage of the FET increases".

Column 8, lines 39 – 33 discuss a read mode operation, in which a memory cell transistor 30 (fig. 3) having the word line and the bit line selected and therefore turned on. In the memory art, it is inherent that word line is connected to the gate of the memory cell, as also clearly indicated in fig. 3, WL to the transistor gate, and the bit line (fig.3 BL) is connected through either a source or a drain. For the instant case, fig. 3 shows that bit line BL is connected to the source. Col. 8, lines 42 – 50 show that a read voltage is applied to the bit line BL_0. Without being mentioned that read voltage is applied to drain-source of the FET, it is nevertheless an inherent feature in the art that voltage applied to bit line, or digit line, of the claimed memory FET, is across the drain-source. As a proof, Fig. 8 shows the memory transistors having bit line signal applied across the drain and the source of the memory transistors.

Furthermore, in the field of transistor design, it is considered inherent that within an operational bias range of a given FET, the current through the drain-source increases as the voltage applied across the drain-source increases. Therefore, with all of the features disclosed in the reference by Taira, it would be considered inherent for one skilled in the memory art, to anticipate the limitations claimed.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham LP

December 4, 2002

David Nelms
Supervisory Patent Examiner
Technology Center 2800